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Sheet 1 of 1

Complete if Known

Application Number	10/631,824
Filing Date	August 1, 2003
First Named Inventor	Xavier Montagne
Art Unit	3705-2819
Examiner Name	TBA Matthew C Tabler
Attorney Docket Number	003921.00143

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
/M.T./		US- 6,473,726	10-29-2002	Reblewski	
/M.T./		US-6,265,894	07-24-2001	Reblewski et al.	
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FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ³
		Country Code ² - Number ⁴ - Kind Code ⁵ (if known)				
/M.T./		WO 94/06210	03-17-1994	Prabhakar Goel		
/M.T./		EP 0 651 343	05-03-95	Quickturn Systems, Inc.		

NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
/M.T./		CHARLES CLOS, "A Study of Non-Blocking Switching Networks", The Bell System Technical Journal, March 1953, pages 406-424	
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/M.T./		Xilinx, "Programmable Gate Array Design Handbook", First Edition, 1986, pages I-A10	
/M.T./		JONATHAN BABB, et al., "Logic Emulation with Virtual Wires", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, June 1997, pages 1-20	

Examiner Signature	/Matthew Tabler/	Date Considered	08/22/2007
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